

FIG. 1

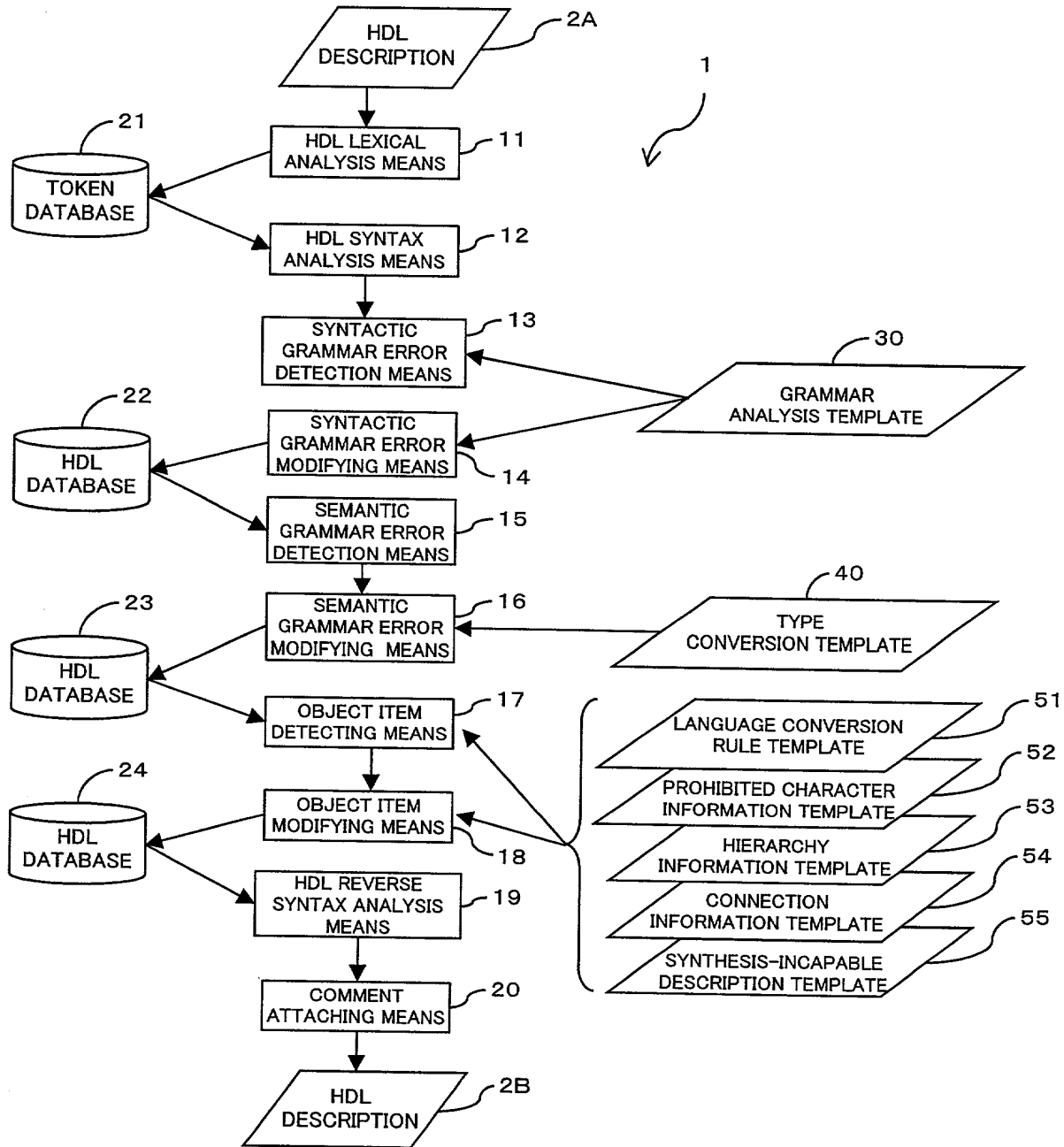
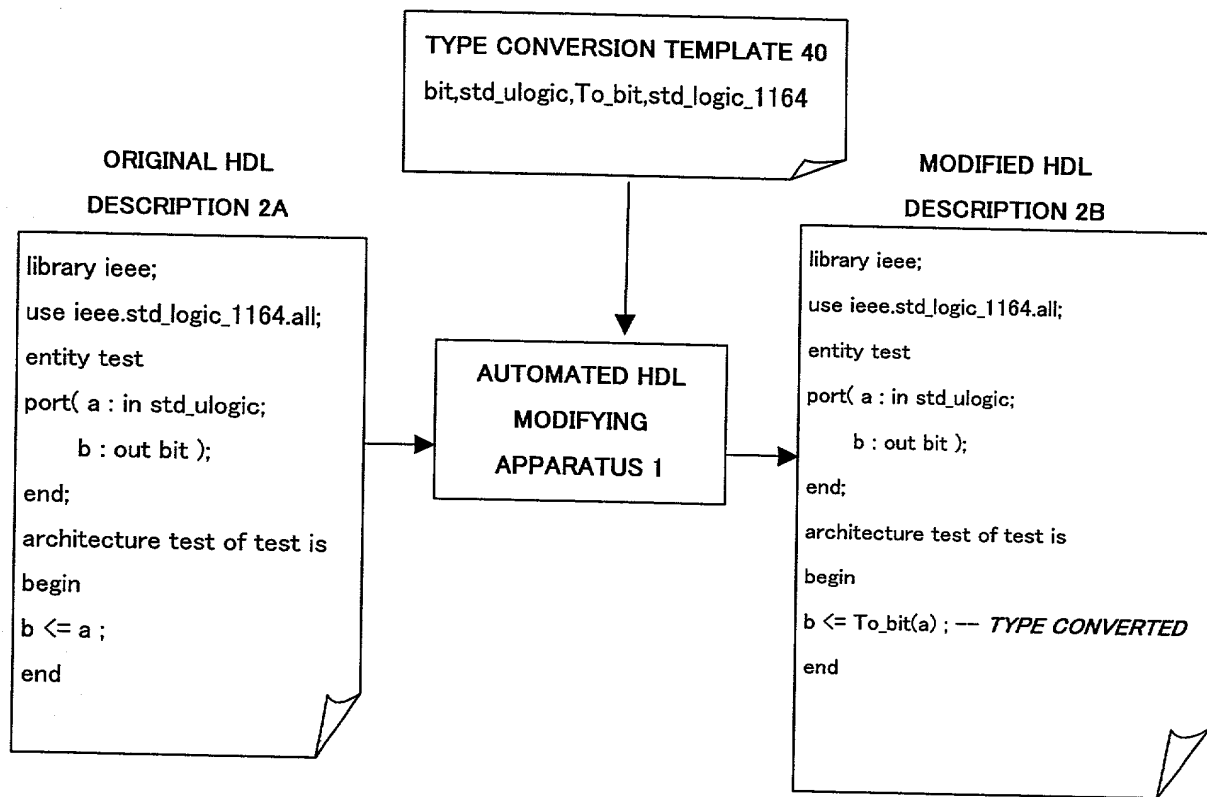


FIG. 2



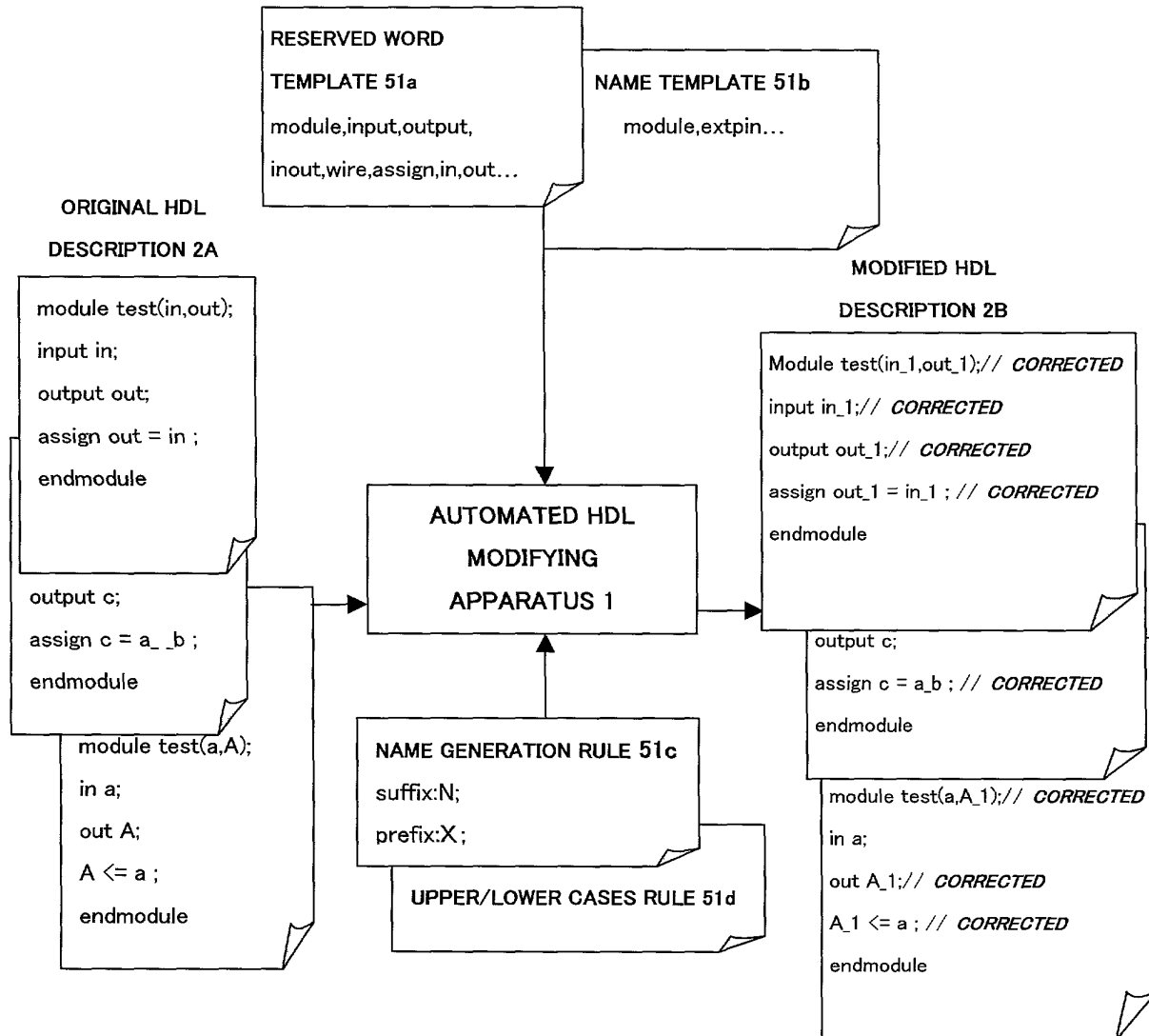
[illegible]

FIG. 4

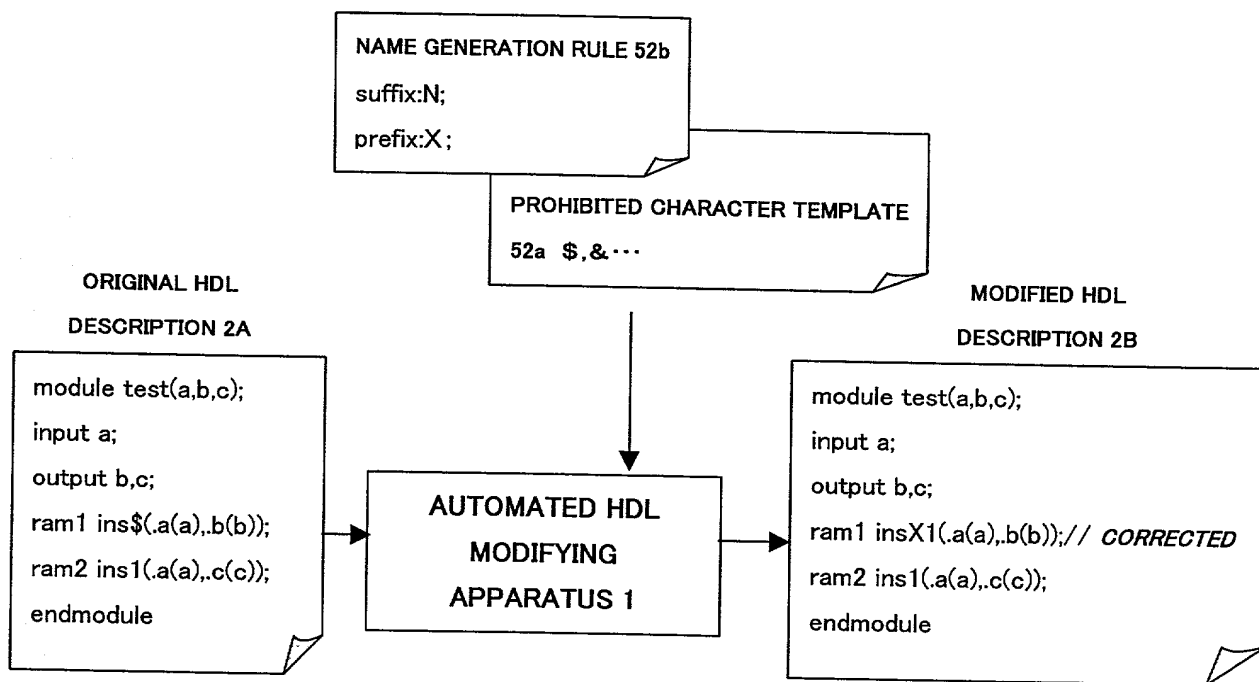


FIG. 5

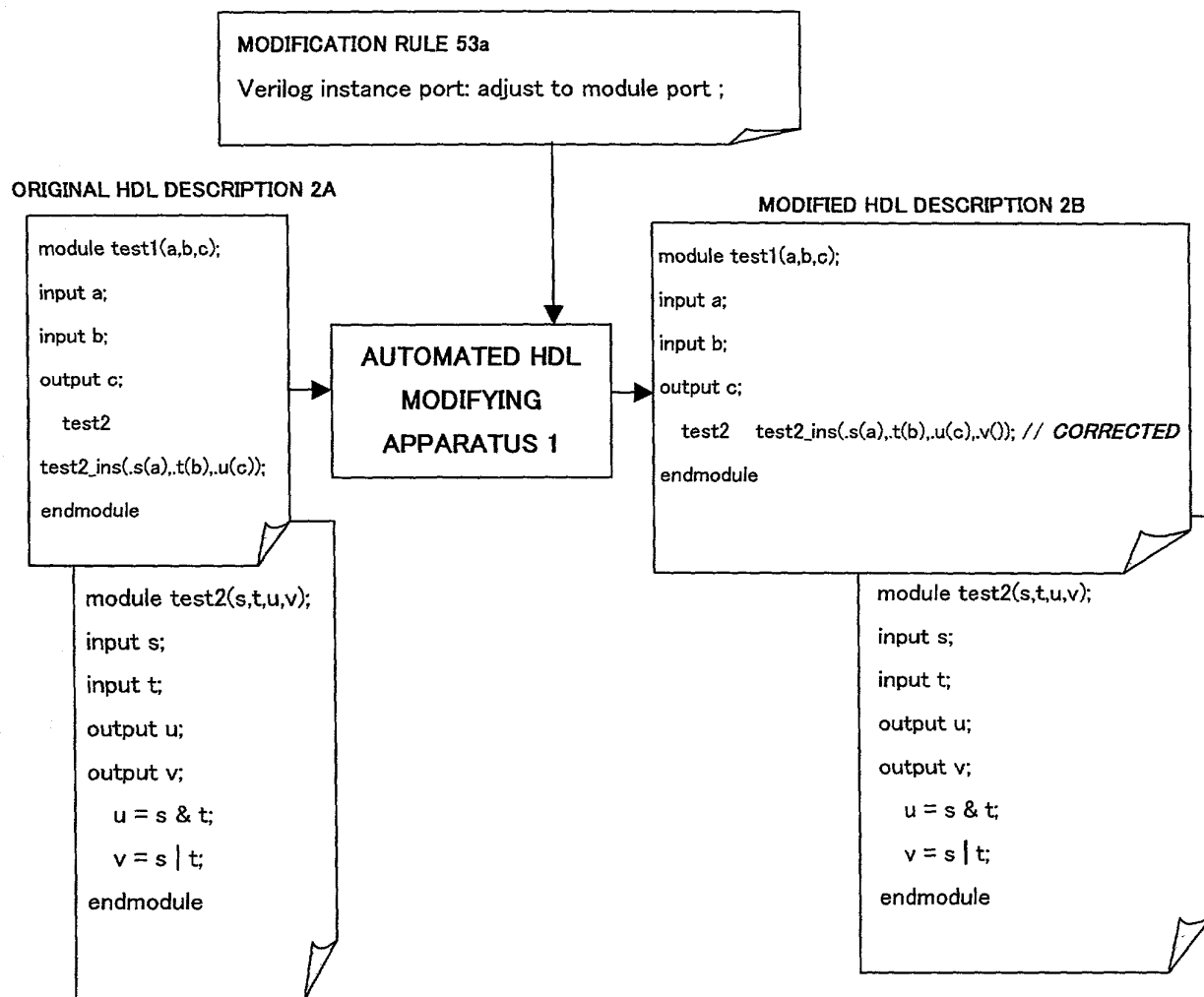


FIG. 6

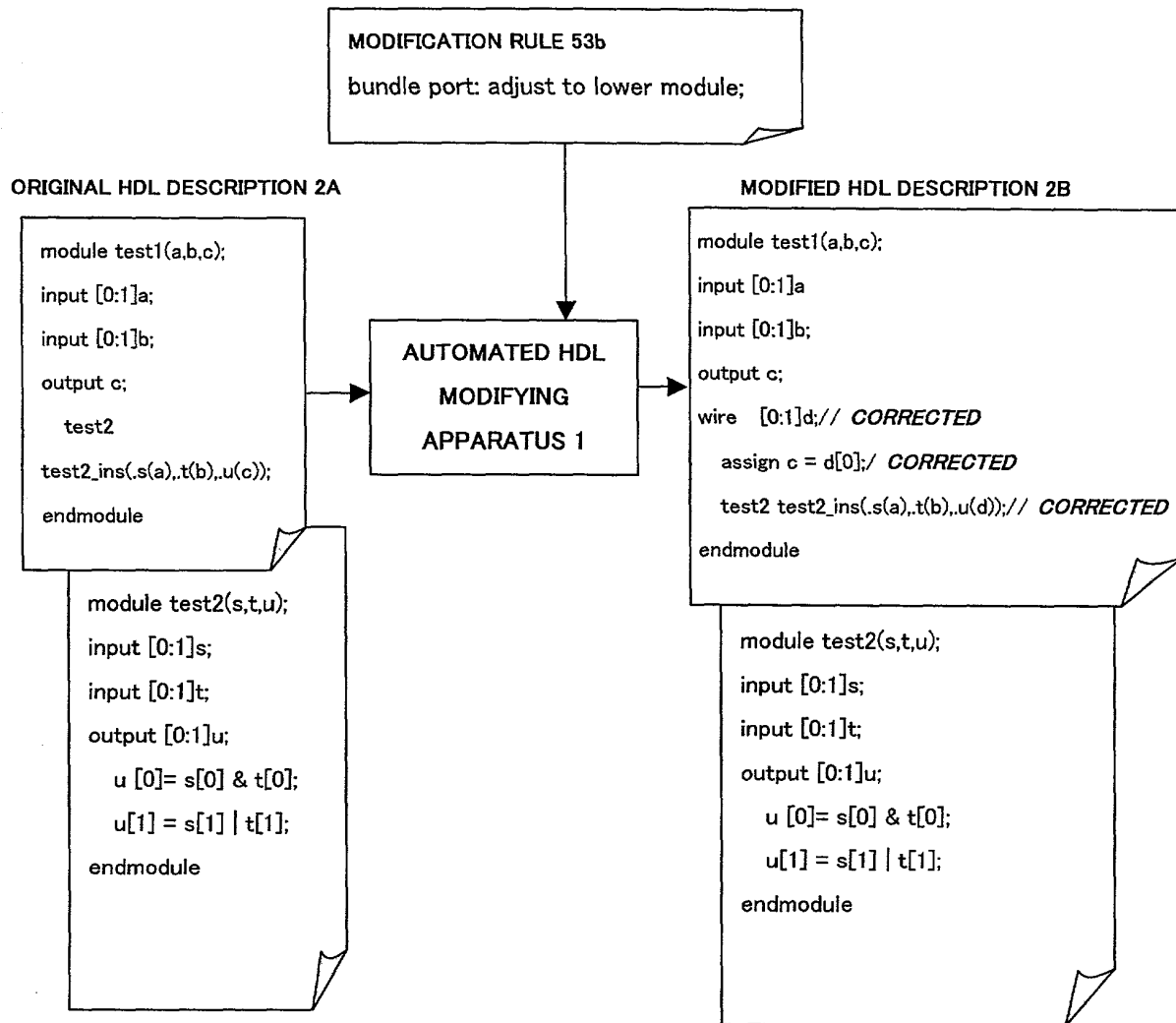


FIG. 7

MODIFICATION RULE 53c

component port: complement to entity;

ORIGINAL HDL DESCRIPTION 2A

```
library IEEE;
use IEEE.std_logic_1164.all;
entity TEST1 is
  port ( A, B : in std_logic;
        C : out std_logic);
end TEST1;
architecture SAMPLE of TEST1 is
  component TEST2
    port (S,T : in std_logic;
          U : out std_logic);
  end component;
begin
  T2: TEST2 port map( S=>A,
T=>B,U=>C);
end;
```

```
library IEEE;
use IEEE.std_logic_1164.all;
entity TEST2 is
  port (S,T : in std_logic;
        U,V : out std_logic);
end TEST2;
architecture SAMPLE of TEST2 is
begin
  U <= S and T;
  V <= S or T;
end;
```

AUTOMATED HDL MODIFYING APPARATUS 1

MODIFIED HDL DESCRIPTION 2B

```
library IEEE;
use IEEE.std_logic_1164.all;
entity TEST1 is
  port ( A, B : in std_logic;
        C : out std_logic);
end TEST1;
architecture SAMPLE of TEST1 is
  component TEST2
    port (S,T : in std_logic;
          U,V : out std_logic);// CORRECTED
  end component;
begin
  T2: TEST2 port map( S=>A,
T=>B,U=>C,V=>OPEN);// CORRECTED
end;
```

```
library IEEE;
use IEEE.std_logic_1164.all;
entity TEST2 is
  port (S,T : in std_logic;
        U,V : out std_logic);
end TEST2;
architecture SAMPLE of TEST2 is
begin
  U <= S and T;
  V <= S or T;
end;
```

FIG. 8

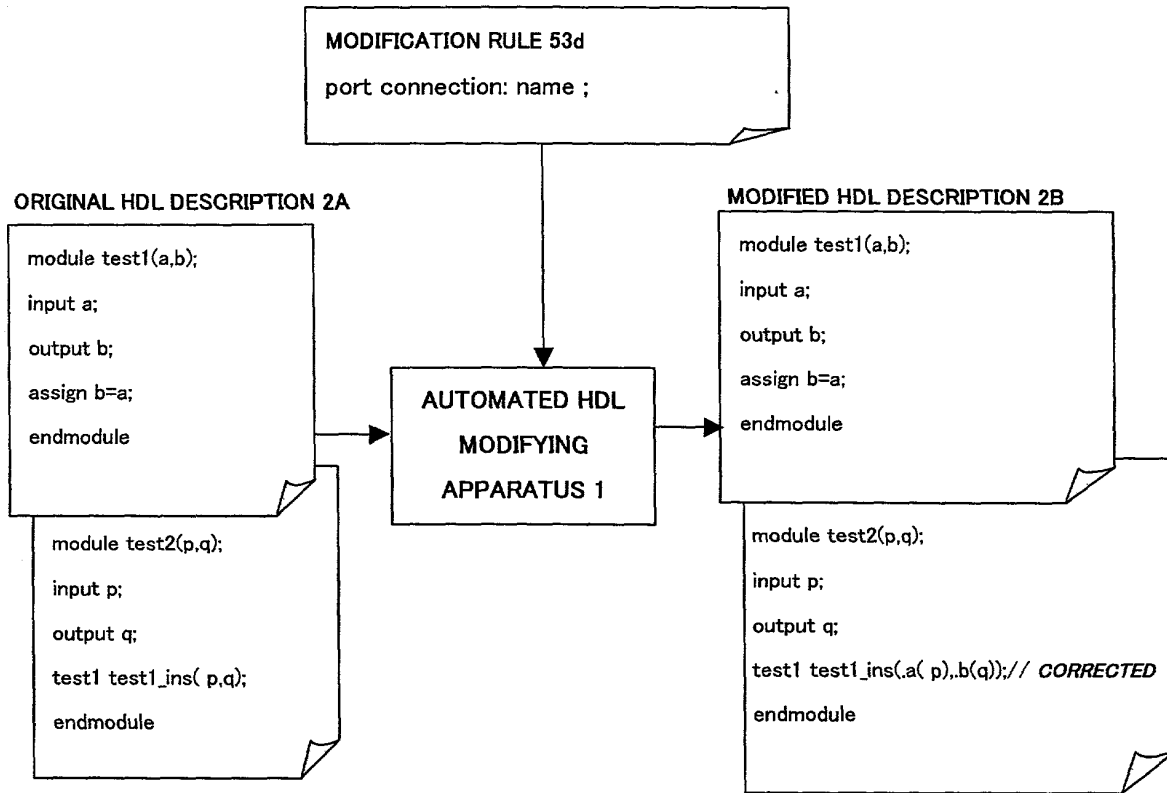


FIG. 9

